Notice of Allowability	Application No. 10/707,971	Applicant(s) DREIBELBIS ET AL.	
	Examiner Cynthia Britt	Art Unit 2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to _6/12/07_.
2. ☒ The allowed claim(s) is/are _1-20, 22-29 and 31-35 (now renumbered 1-33)_.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

CYNTHIA BRITT
PRIMARY EXAMINER
2-11-08

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Pam Riley on 2/4/08.

The application has been amended as follows:

Claims are to be amended as follows:

1. (Currently Amended) A hybrid built-in self test (BIST) architecture for embedded memory arrays that segments BIST functionality into remote lower-speed executable instructions and local higher-speed executable instructions, the architecture comprising:

a BIST logic controller that is separate from said embedded memory arrays, ~~is adapted to operate~~ said BIST logic controller operates at a lower frequency than said embedded memory arrays~~,~~ and ~~is further adapted to~~ performs test functions common to all of said embedded memory arrays at said lower frequency; and

a plurality of blocks of test logic in communication with said BIST logic controller,

~~wherein~~ each one of said blocks is incorporated into a corresponding one of said embedded memory arrays under test~~, is adapted to~~

said each one of said blocks operates at a same frequency as said corresponding one of said embedded memory arrays, said same frequency comprising a higher frequency relative to

said frequency of said BIST logic controller, ~~and is further adapted to~~

said each one of said blocks performs test functions unique to said corresponding one of said embedded memory arrays at said same frequency,

~~wherein said same frequency comprises a higher frequency relative to said lower frequency of said BIST logic controller,~~

~~wherein~~ said BIST logic controller ~~is~~ further ~~adapted to~~ communicates, to said each one of said blocks of test logic, instructions at said lower frequency, and

~~wherein said each of~~ said each one of said blocks ~~is~~ further ~~adapted to~~ locally processes said instructions at said higher frequency.

2. (Currently Amended) The hybrid BIST architecture in claim 1, ~~wherein~~ said each one of said blocks of test logic ~~each comprise~~ comprising a multiplier for increasing the frequency of said instructions from said lower frequency to said higher frequency.

3. (Currently Amended) The hybrid BIST architecture in claim 1, ~~wherein~~ said each one of said blocks of test logic comprising ~~comprises~~:

a clock multiplier;

redundancy allocation logic;

data address control generation logic; and

decoding logic that ~~adapted to~~ decodes each of said instructions received from said BIST logic controller into multiple individual micro-instructions that are tailored to said corresponding one of said embedded memory arrays, and

~~wherein~~ said data address control generation logic and said redundancy allocation logic using ~~are~~

~~adapted to use~~ said micro-instructions to perform data address control generation and redundancy allocation, respectively, based on said micro-instructions.

4. (Currently Amended) The hybrid BIST architecture in claim 1, ~~wherein~~ said BIST logic controller in combination with said blocks of test logic enabling ~~enables~~ in parallel testing of at least one of the following:

different types of embedded memories, ~~wherein~~ said different types comprising ~~comprise~~ at least one of a dynamic random access memory (DRAM) array, a static random access memory (SRAM) array, and a content-addressable memory (CAM) array;

memory arrays operating at different frequencies; and

different size memory arrays.

5. (Previously Presented) The hybrid BIST architecture in claim 1, further comprising a lower-speed control bus operating at said lower frequency and connecting said BIST logic controller to said blocks so as to allow communication of said instructions from said BIST logic controller to said blocks.

6. (Currently Amended) The hybrid BIST architecture in claim 1, ~~wherein~~ said BIST logic controller comprising ~~comprises~~ at least one of a read only memory (ROM), a scannable read only memory (SROM), and other type of memory ~~adapted to~~ that stores macro instruction sets.

7. (Currently Amended) The hybrid BIST architecture in claim 1, ~~wherein~~ said BIST logic controller comprising ~~comprises~~ logic ~~adapted to~~ that provides branch prediction, program

counter management, utility counters, and general BIST operation controls and diagnostic outputs.

8. (Currently Amended) A built-in self test (BIST) architecture for use with embedded memory arrays in functional circuitry within an integrated circuit, said BIST architecture comprising:

a BIST logic controller that is separate from said embedded memory arrays, ~~is adapted to~~ said BIST logic controller operates at a lower frequency than said embedded memory arrays~~,~~ and ~~is further adapted to~~ performs test functions common to all of said embedded memory arrays at said lower frequency;

a plurality of blocks of test; and

a bus connecting said BIST logic controller to each one of said blocks of test logic so as to allow communication from said BIST logic controller to said blocks,

~~wherein~~ said bus ~~is adapted to~~ operates at said lower frequency,

~~wherein~~ said each one of said blocks is incorporated into a corresponding one of said embedded memory arrays,

said each one of said blocks ~~is adapted to~~ operates at a same frequency as said corresponding one of said embedded memory arrays, said same frequency comprising a higher frequency relative to said frequency of said BIST logic controller and said bus,

said each one of said blocks ~~and is~~ further ~~adapted to~~ performs test functions unique to said corresponding one of said embedded memory arrays,

~~wherein said same frequency comprises a higher frequency relative to said lower~~

~~frequency of said BIST logic controller and said bus,~~

~~wherein~~ said BIST logic controller ~~is~~ further ~~adapted to~~ communicates, to said each one of said blocks, instructions at said lower frequency via said bus, and

~~wherein~~ said each one of said blocks ~~is~~ further ~~adapted to~~ locally processes said instructions at said higher frequency.

9. (Currently Amended) The BIST architecture in claim 8, ~~wherein~~ said each one of said blocks of test logic ~~each comprise~~ comprising a multiplier for increasing the frequency of said instructions from said lower frequency to said higher frequency.

10. (Currently Amended) The BIST architecture in claim 11, ~~wherein~~ said data address control generation logic and said redundancy allocation logic using ~~are adapted to use~~ said micro-instructions to perform data address control generation and redundancy allocation, respectively, based on said micro-instructions.

11. (Currently Amended) The BIST architecture in claim 8, ~~wherein~~ said each one of said blocks of test logic comprising ~~comprises~~:

a clock multiplier;

redundancy allocation logic;

data address control generation logic; and

decoding logic ~~adapted to~~ that decodes each of said instructions received from said BIST logic controller into multiple individual micro-instructions that are tailored to said corresponding

one of said embedded memory arrays.

12. (Currently Amended) The BIST architecture in claim 8, ~~wherein~~ said BIST logic controller in combination with said blocks of test logic enabling ~~enables~~ in parallel testing of at least one of the following:

different types of embedded memories, ~~wherein~~ said different types comprising ~~comprise~~ at least one of a dynamic random access memory (DRAM) array, a static random access memory (SRAM) array, and a content-addressable memory (CAM) array;

memory arrays operating at different frequencies; and

different size memory arrays.

13. (Currently Amended) The BIST architecture in claim 8, ~~wherein~~ said BIST logic controller ~~comprises~~ comprising at least one of a read only memory (ROM), a scannable read only memory (SROM), and other type of memory ~~adapted to~~ that stores macro instruction sets.

14. (Currently Amended) The BIST architecture in claim 8, ~~wherein~~ said BIST logic controller comprising ~~comprises~~ logic ~~adapted to~~ that provides branch prediction, program counter management, utility counters, and general BIST operation controls and diagnostic outputs.

15. (Currently Amended) A built-in self test (BIST) architecture for use with embedded memory arrays in functional circuitry within an integrated circuit, said BIST architecture comprising:

a BIST logic controller that is separate from said embedded memory arrays, ~~is adapted to~~ said BIST logic controller operates~~,~~ at a lower frequency than said embedded memory arrays~~,~~ and ~~is further adapted to~~ performs test functions common to all of said embedded memory arrays at said lower frequency;

a plurality of blocks of test logic; and

a bus connecting said BIST logic controller to ~~said~~ each one of said blocks of test logic so as to allow communication from said BIST logic controller to said blocks,

~~wherein~~ said bus ~~is adapted to~~ operates at said lower frequency,

~~wherein~~ said each one of said blocks of test logic is incorporated into a corresponding one of said embedded memory arrays,

said each one of said blocks of test logic ~~is adapted to~~ operates at a same frequency as said corresponding one of said embedded memory arrays, said same frequency is a higher frequency relative to said lower frequency of said BIST logic controller and said bus,

said each one of said blocks of test logic ~~and is~~ further ~~adapted to~~ performs test functions unique to said corresponding one of said embedded memory arrays,

~~wherein said same frequency is a higher frequency relative to said lower frequency of said BIST logic controller and said bus,~~

~~wherein~~ said BIST logic controller ~~is~~ further ~~adapted to~~ communicates, to said each one of said blocks of test logic, instructions at said lower frequency via said bus,

~~wherein~~ said each one of said blocks of test logic ~~is~~ further ~~adapted to~~ locally processes said instructions at said higher frequency, and

~~wherein~~ said test functions that are common to all of said embedded memory arrays

comprise providing branch prediction, program counter management, utility counting, and general BIST operation control and diagnostic outputs.

16. (Currently Amended) The BIST architecture in claim 15, ~~wherein~~ said each one of said blocks of test logic ~~each comprise~~ comprising a multiplier for increasing the frequency of said instructions from said lower frequency to said higher frequency.

17. (Currently Amended) The BIST architecture in claim 18, ~~wherein~~ said data address control generation logic and said redundancy allocation logic using ~~are adapted to~~ ~~use~~ said micro-instructions to perform data address control generation and redundancy allocation, respectively, based on said micro-instructions.

18. (Currently Amended) The BIST architecture in claim 15, ~~wherein each of~~ said each one of said blocks of test logic comprising ~~comprises~~:

a clock multiplier;

redundancy allocation logic;

data address control generation logic; and

decoding logic that ~~adapted to~~ decodes each of said instructions received from said BIST logic controller into multiple individual micro-instructions that are tailored to said corresponding one of said embedded memory arrays.

19. (Currently Amended) The BIST architecture in claim 15, ~~wherein~~ said BIST logic controller in combination with said blocks of test logic enabling ~~enables~~ in parallel testing of at

least one of the following:

different types of embedded memories, wherein said different types comprise at least one of a dynamic random access memory (DRAM) array, a static random access memory (SRAM) array, and a content-addressable memory (CAM) array;

memory arrays operating at different frequencies; and

different size memory arrays.

20. (Currently Amended) The BIST architecture in claim 15, ~~wherein~~ said BIST logic controller ~~comprises~~ comprising at least one of a read only memory (ROM), a scannable read only memory (SROM), and other type of memory ~~adapted to~~ that stores macro instruction sets.

21. (Cancelled).

22. (Currently Amended) A method of testing embedded memory arrays in functional circuitry within an integrated circuit using a built-in self test (BIST) architecture, said method comprising:

performing, by a BIST logic controller, test functions common to all of said embedded memory arrays[[,]]

~~wherein~~ said BIST logic controller ~~is~~ being remote from said embedded memory arrays and operating ~~operates~~ at a lower frequency than said embedded memory arrays;

sending, by said BIST logic controller, instructions to a plurality of blocks of test logic,

~~wherein~~ each one of said blocks being ~~is~~ incorporated into a corresponding one of said embedded memory arrays and ~~operates~~ operating at a same frequency as said corresponding one

of said embedded memory array, ~~and wherein~~ said same frequency ~~comprises~~ comprising a higher frequency relative to said lower frequency of said BIST logic controller; and

performing, by said each one of said blocks, test functions unique to said corresponding one of said embedded memory arrays, ~~wherein~~ said performing comprising ~~comprises~~:

increasing the frequency of said instructions to said higher frequency.

23. (Currently Amended) The method in claim 22, ~~wherein~~ said sending comprising ~~comprises~~ using a bus connecting said BIST logic controller to said blocks of test logic so as to allow communication of said instructions from said BIST logic controller to said blocks, wherein said bus operates at said lower frequency of said BIST logic controller.

24. (Currently Amended) The method in claim 25, ~~wherein~~ said performing of data address control generation and said performing of said redundancy allocation ~~are~~ being based on said individual micro-instructions.

25. (Currently Amended) The method in claim 22, ~~wherein~~ said performing, by said each one of said blocks, comprising ~~comprises~~:

performing redundancy allocation;

performing data address control generation; and

decoding each of said instructions received from said BIST logic controller into individual micro-instructions that are tailored to said corresponding one of said embedded memory arrays.

26. (Currently Amended) The method in claim 22, ~~wherein~~ said performing by said BIST logic controller of said test functions common to all of said embedded memory arrays and said performing by said each of said blocks of said test functions unique to said corresponding one of said embedded memory arrays ~~enables~~ enabling in parallel testing of at least one of the following:

different types of embedded memories, ~~wherein~~ said different types comprising ~~comprise~~ at least one of a dynamic random access memory (DRAM) array, a static random access memory (SRAM) array, and a content-addressable memory (CAM) array;

memory arrays operating at different frequencies; and

different size memory arrays.

27. (Currently Amended) The method in claim 22, further comprising storing said instructions in one of read only memories (ROMs), a scannable read only memory (SROM), and other type of memory in said BIST logic controller.

28. (Currently Amended) The method in claim 22, ~~wherein~~ said performing by said BIST logic controller of said test functions common to all of said embedded memory arrays ~~comprises~~ comprising performing:

branch prediction;

program counter management;

utility counting; and

general BIST operation control and diagnostic outputs.

29. (Currently Amended) A method of testing embedded memory arrays in functional circuitry within an integrated circuit using a built-in self test (BIST) architecture, said method comprising:

performing, by a BIST logic controller, test functions common to all of said embedded memory arrays,

~~wherein~~ said BIST logic controller ~~is~~ being separate from said embedded memory arrays and ~~operates~~ operating at a lower frequency than said embedded memory arrays;

sending, by said BIST logic controller, instructions a plurality of blocks of test logic,

~~wherein~~ said sending comprising ~~comprises~~ using a bus connecting said BIST logic controller to said blocks of test logic so as to allow communication from said BIST logic controller to said blocks,

~~wherein~~ said bus ~~operates~~ operating at said lower frequency of said BIST logic controller,

~~wherein~~ each one of said blocks ~~is~~ being incorporated into a corresponding one of said embedded memory arrays and ~~operates~~ operating at a same frequency as said corresponding one of said embedded memory arrays,

~~wherein~~ said same frequency ~~comprises~~ comprising a higher frequency relative to said lower frequency of said BIST logic controller and said bus; and

performing, by each of said blocks, test functions unique to said corresponding one of said embedded memory arrays, ~~wherein~~ said performing comprising ~~comprises~~:

increasing the frequency of said instructions to said higher frequency.

30. (Cancelled).

31. (Currently Amended) The method in claim 32, ~~wherein~~ said performing of data address control generation and said performing of said redundancy allocation being ~~are~~ based on said individual micro-instructions.

32. (Currently Amended) The method in claim 29, ~~wherein~~ said performing, by each of said blocks, comprising ~~comprises~~:

performing redundancy allocation;

performing data address control generation; and

decoding each of said instructions received from said BIST logic controller into individual micro-instructions that are tailored to said corresponding one of said embedded memory arrays.

33. (Currently Amended) The method in claim 29, ~~The method in claim 22, wherein~~ said performing by said BIST logic controller of said test functions common to all of said embedded memory arrays and said performing by said each of said blocks of said test functions unique to said corresponding one of said embedded memory arrays enable ~~enables~~ in parallel testing of at least one of the following:

different types of embedded memories, ~~wherein~~ said different types comprising ~~comprise~~ at least one of a dynamic random access memory (DRAM) array, a static random access memory (SRAM) array, and a content-addressable memory (CAM) array;

memory arrays operating at different frequencies; and

different size memory arrays.

34. (Currently Amended) The method in claim 29, further comprising storing said instructions in one of read only memories (ROMs), a scannable read only memory (SROM), and other type of memory in said BIST logic controller.

35. (Currently Amended) The method in claim 29, ~~wherein~~ said performing by said BIST logic controller of said test functions common to all of said embedded memory arrays ~~comprises~~ comprising performing:

branch prediction;

program counter management;

utility counting; and

general BIST operation control and diagnostic outputs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner
Art Unit 2117

Cynthia Britt

CYNTHIA BRITT
PRIMARY EXAMINER

2-4-08